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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,458	01/15/2004	Michael Vlasov	0120128	5874

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EXAMINER	
BRINEY III, WALTER F	
ART UNIT	**PAPER NUMBER**
2646	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,458	VLASOV ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hershbarger (US Patent Application Publication 2004/0239487) in view of Dong et al. (US Patent Application Publication 2003/0215020).**

Claim 1 is limited to *an isolation barrier coupled between a system side device and a line side device.* Hershbarger discloses a method and apparatus for full duplex signaling across a transformer. See Abstract. With respect to figure 1: the host interface component (104) corresponds to the *system side device*, the line interface component (106) corresponds to the *line side device*, and the isolation barrier (106) comprising a pulse transformer corresponds to the *isolation barrier comprising a transformer.* See paragraphs 36-39. With respect to figure 10: the rectifier (1002) controls a MOSFET that corresponds to a *controlled impedance.* In operation, the HIC is either transmitting or receiving (i.e. in a transmit mode or receive mode). In the transmit mode, the HIC modulates a transmitted clock signal, and predictably, transmits the clock signal without modulation during the receive mode. See the signaling section beginning in paragraph 70 for a description of transmission. The LIC transmits data in accordance with data from the subscriber loop by modulating the impedance presented

to the clock signals transmitted by the HIC. See Abstract. As the transformer is the only means for transmitting clock, power and data between the HIC and LIC, it is inherent that the transformer is configured to provide the modulated clock signal to the line side device (LIC) from the system side device (HIC) and to provide the clock signal amplitude modulated by the controlled impedance to the system side device (HIC) from the line side device (LIC). However, the Manchester encoding scheme of Hershbarger does not meet the limitations of the system side device as recited, which is configured to generate an amplitude modulated clock signal.

Dong teaches a data access arrangement using a high frequency transformer for electrical isolation. In part, Dong teaches the specific drawbacks of using a pulse transformer in isolation. See the section entitled Summary of the Invention, paragraphs 11-14. In solution, Dong teaches replacing the prior art pulse transmitter and transformer with a high-frequency transmitter and transformer, where the high-frequency transmitter amplitude modulates a transmitted clock signal with data to be transmitted.

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace a pulse transmitter and pulse transformer with the high-frequency transmitter and high-frequency transformer as taught by Dong for the purpose of reducing costs and enabling linear data transmission.

Claim 2 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. Hershbarger discloses a decoder (618) as seen in figure 6 that uses a threshold detector, which corresponds to a *comparator*, for decoding receive data RXD

that modulates the transmitted clock signal. See paragraphs 86 and 87. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 3 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. Hershbarger discloses providing power to the line interface component (LIC), which corresponds to the line side device, using a clock signal. This is illustrated in figure 7 where periods of power distribution result in much higher base amplitudes. In this way, the clock generator/transmitter of the HIC inherently corresponds to a power-clock driver. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 4 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. As seen in figure 1 of Hershbarger, any signals transmitted by the HIC to the LIC will provide power, including said amplitude modulated clock signal. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 5 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. As seen in figure 1 of Hershbarger, any signals transmitted by the HIC to the LIC will provide power, including said unmodulated clock signal. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 6 is limited to *the isolation barrier of claim 5*, as covered by Hershbarger in view of Dong. Hershbarger discloses modulating the impedance of the transistor seen in figure 10 to transmit data from the LIC. See paragraph 56. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 7 is limited to *the isolation barrier of claim 3*, as covered by Hershbarger in view of Dong. As previously discussed in the rejection of claim 1, the clock signal is amplitude modulated to provide data to the LIC. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 8 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. As seen in figure 10 of Hershbarger the controlled impedance element comprises a MOSFET. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 9 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. It is an inherent property of the transformer taught by Dong that noise is prevented from passing between the LIC and HIC. Furthermore, Dong teaches in the Summary of the Invention that harmonics are removed by the high-frequency modulation scheme. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claim 10 is limited to *the isolation barrier of claim 1*, as covered by Hershbarger in view of Dong. It is an inherent property of a transformer that ground changes in the LIC will not cause a ground change in the HIC because the grounds are physically isolated. Therefore, Hershbarger in view of Dong makes obvious all limitations of the claim.

Claims 11-16 recite various elements of claim 1, as covered by Hershbarger in view of Dong, and are rejected for the same reasons, respectively.

Claims 17-20 recite essentially the same elements of claims 2-5, as covered by Hershbarger in view of Dong, and are rejected for the same reasons, respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SINH TRAN
SUPERVISORY PATENT EXAMINER

WFB
10/14/05